This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-3. (Cancelled)

4. (Currently Amended) The method of Claim 40 wherein the first ion implanting step of the p-type or n-type dopants is ion implanting the p-type dopant in which the p-type dopant is selected from the group consisting of Ga, Al, B and BF_2.

5. (Original) The method of Claim 4 wherein the p-type dopant is B, said B is implanted at an energy of from about 100 keV to about 500 keV and a dose of about 5E15 atoms/cm^2 to about 5E16 atom/cm^2.

6. (Original) The method of Claim 4 wherein the p-type dopant is BF_2, said BF_2 is implanted at an energy of from about 500 keV to about 2500 keV and a dose of about 5E15 atoms/cm^2 to about 5E16 atom/cm^2.

7. (Cancelled)

8. (Previously presented) The method of Claim 40 wherein the annealing comprises a furnace anneal, a rapid thermal anneal, or a spike anneal.

9. (Original) The method of Claim 8 wherein the annealing is a furnace anneal step, said furnace anneal step is carried out at a temperature of about 600°C or greater for a time period of about 15 minutes or greater in the presence of an inert gas atmosphere, an oxidizing ambient or a mixture thereof.

10. (Original) The method of Claim 8 wherein the annealing is a rapid thermal anneal (RTA) step, said RTA step is carried out at a temperature of about 800°C or greater for a time period of

about 5 minutes or less in the presence of an inert gas atmosphere, an oxidizing ambient or a mixture thereof.

11. (Original) The method of Claim 8 wherein the annealing is a spike annealing step, said spike annealing step is performed at a temperature of about 900°C or greater for a time period of about 1 second or less in the presence of an inert gas atmosphere, an oxidizing ambient or a mixture thereof.

12.-15. (Cancelled)

16. (Previously Presented) The method of Claim 40 further comprising forming a cap layer atop the Si-containing substrate after said electrolytic anodization process, but prior to said oxidizing.

17. (Original) The method of Claim 16 wherein the cap layer comprises a Si-containing material.

18. (Previously Presented) The method of Claim 40 wherein the thermal oxidizing is performed in an oxygen-containing ambient.

19. (Original) The method of Claim 18 wherein the oxygen-containing ambient further comprises an inert gas.

20. (Original) The method of Claim 19 wherein the oxygen-containing ambient is selected from the group consisting of O_2, NO, N_2O, ozone, and air.

21. (Previously Presented) The method of Claim 40 wherein the thermal oxidizing is performed at a temperature of from about 1200°C to about 1325°C.

22. (Previously Presented) The method of Claim 40 wherein the thermal oxidizing forms a surface oxide atop the Si-containing over-layer.

23. (Previously Presented) The method of Claim 40 wherein the buried oxide region is uniform.

24. (Previously Presented) The method of Claim 40 wherein the buried oxide region comprises discrete islands of thermal oxide.

25.-26. (Cancelled)

27. (Previously Presented) The method of Claim 40 further comprising a pre-oxidization step prior to said thermal oxidizing, said pre-oxidization step includes oxidation in a wet oxygen ambient.

28. (Original) The method of Claim 27 wherein said pre-oxidization step is performed at a temperature from about 600°C to about 1200°C.

29. (Previously Presented) The method of Claim 40 further comprising a post oxidation step, said post oxidation step comprising a thermal anneal in a hydrogen ambient.

30. (Original) The method of Claim 29 wherein the post oxidization step is performed at a temperature from about 900°C to about 1200°C.

31.-33. (Cancelled)

34. (Currently Amended) The method of Claim 40 wherein said at least one ion of said second ion implanting step is Si and said second ion implanting step is performed using a Si dose from about 1E15 to about 1E16 atoms/cm^2 and an implant energy from about 200 to about 500 keV.

35.-38. (Cancelled)

39. (Previously Presented) The method of Claim 40 further comprising patterning the Si-containing substrate prior to the ion implanting of the p-type or n-type dopants into the Si-containing substrate.

40. (Currently Amended) A method of fabricating a silicon-on-insulator substrate comprising:

a first ion implanting step to implant p-type or n-type dopants into a Si-containing substrate to a depth ranging from 250 nm to 1500 nm from a top surface of the Si-containing substrate;

a second ion implanting step following the first ion implanting step to implant ~~implanting~~ at least one ion selected from the group consisting of Si, Ge, Ne, Bi, Sn and Xe, wherein the at least one ion may be implanted to below, above or within the depth at which the p-type or n-type dopants are present in the Si-containing substrate;

annealing the n-type or p-type dopants following the second ion implanting step to provide an activated n-type or p-type dopant region in the Si-containing substrate;

performing an electrolytic anodization process comprising immersing the Si-containing substrate into an HF-containing solution and applying a current density ranging from 0.05 milliAmps/cm^2 to 50 milliAmps/cm^2 to the Si-containing substrate to produce a porous Si region having a porosity of 0.01% or greater at a depth greater than 50 nm from the upper surface of the Si-containing substrate, wherein the electrolytic anodization process converts ~~at least a portion of~~ the activated n-type or p-type dopant region into the porous Si region; and

thermal oxidizing at a temperature ranging from 650°C to 1350°C to convert at least a portion of the porous Si region into a buried oxide region, wherein a portion of the Si-containing substrate overlying the buried oxide region and a remaining portion of the porous Si region coalesces to provide a Si-containing overlayer.